

General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.
- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.
- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.
- This document is paginated as submitted by the original source.
- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

(NASA-CR-174057) RESEARCH ON GALLIUM
ARSENIDE DIFFUSED JUNCTION SOLAR CELLS
Final Report, 1 Oct. 1982 - 30 Jun. 1984
(Rensselaer Polytechnic Inst., Troy, N. Y.)
54 p HC A04/MF A01

N85-11457

Unclas
24391

CSCL 10A G3/44

FINAL REPORT

for

NASA Grant NAG 3-188

entitled

"RESEARCH ON GALLIUM ARSENIDE DIFFUSED JUNCTION SOLAR CELLS"

for the period

October 1, 1982 to June 30, 1984

J. M. Borrego

S. K. Ghandhi
(Co-Principal Investigators)



Electrical, Computer, and Systems Engineering Department

Rensselaer Polytechnic Institute

Troy, New York 12181

October 1984

CONTRIBUTORS

I. Bhat

K. N. Bhat

R. Keeney

G. Mathur

H. Rode

L. M. G. Sundaram

CONTENTS

ABSTRACT.....	4
1. INTRODUCTION.....	5
2. WORK PERFORMED ON THIS PROGRAM.....	5
2.1 Cell Fabrication.....	5
2.1.1 <u>Starting n-GaAs</u>	6
2.1.2 <u>Junction Formation</u>	7
2.1.3 <u>Contacts and Patterning</u>	12
2.1.4 <u>Anti-Reflective Coating</u>	13
2.1.5 <u>Alternate Cell Fabrication</u>	14
2.2 Electrical Characterization and Device Simulation....	14
2.2.1 <u>Electrical Measurements</u>	15
2.2.2 <u>Solar Cell Measurements</u>	16
2.2.3 <u>Computer Simulation of Spectral Response</u>	17
3. EDUCATIONAL AND PROFESSIONAL.....	18
4. CONCLUDING SUMMARY.....	19

ABSTRACT

This program was initiated with the award of a 3-month grant to begin work on the feasibility of using bulk GaAs, in conjunction with open tube diffusion techniques, for the fabrication of solar cells. This was followed by a 12-month renewal phase, from October 1, 1981 to September 30, 1982. The next renewal was for the period October 1, 1982 to December 31, 1983, with an extension to June 30, 1984. This report covers these periods and summarizes our work on this program.

During this period, we have demonstrated an AM0 efficiency of 12.8% that can be achieved at 1 sun illumination, using these techniques. Moreover, extensive device characterization, combined with the development of a computer model, has predicted that cell efficiencies approaching 20% can be obtained by suitable process and design changes, and by the availability of slightly improved starting material.

A number of papers and presentations have been made on our work in this area. These are listed in Section 3 of this report.

1. INTRODUCTION

The goal of this program is to determine the feasibility of using bulk GaAs for the fabrication of diffused-junction solar cells, to study the effects of thermal processing of GaAs, and to assess the quality of starting bulk GaAs for this purpose. These cells are to be made by open-tube diffusion techniques, and are to be tested for photovoltaic response under AMO conditions. This report describes work accomplished during the last reporting period, and summarizes work done over the grant period towards meeting this goal.

2. WORK PERFORMED ON THIS PROGRAM

The work on this program can be divided into two parts. The first of these is concerned with aspects of cell fabrication, beginning with the substrate, and leading to the complete cell structure. The second deals with electrical characterization, and covers basic measurements to determine equivalent circuit parameters, computer modelling for simulation of cell behavior, and photovoltaic measurements to determine cell performance. The work in the characterization effort provided guidelines for modifying the cell fabrication process, and thus gave the necessary feedback for an integrated program on this subject.

2.1 Cell Fabrication

This basic cell concept is a simple one, since the thrust of the program was to study the feasibility of using bulk GaAs for the fabrication of low cost cells. The cell structure consists of a single p^+ -diffusion into bulk GaAs. This is followed by ohmic contact formation to the back side, and by photo-delineation of the active cell

pattern. A relatively simple AR coating is used to form the completed cell structure. Each of these aspects is now considered in detail.

2.1.1 Starting n-GaAs:

There are many vendors for this material, which is available in a variety of dopants, and is grown by different methods. However, the choice was narrowed down as follows:

- (a). Only (100) orientation was considered. This is the primary orientation used for starting material by device manufacturers and so is available with the broadest range of options.
- (b). Originally, we restricted our work to Liquid Encapsulated Czochralski material. Here, we found results somewhat variable, i.e., some source material was very good and some was very bad. This, we believe, is an indicator of the changing art in this area, where considerable progress is being made at the present time. Bridgman material, on the other hand, was found to be generally consistent; again, this is probably due to the maturity of this type of process. Consequently, we have used this material as well in our work. Epitaxial layers, grown by the organometallic process, were also used in this program. Primarily, this material was used for the purposes of carrying out controlled experiments for diagnostic purposes. Some solar cells were fabricated on this material to provide a basis of comparison with cells diffused in bulk GaAs.

(c). Slices used on this program were doped with Selenium, Tellurium, Silicon and Tin. Very little work was done with the tin-doped material, primarily because we found it gave consistently poor results; moreover, it was not available from multiple sources.

(d). Our biggest problem was in the area of doping level. As-purchased, bulk GaAs is either heavily doped, or is semi-insulating. For solar cell applications, it is desirable to have material in the $1-5 \times 10^{16}/\text{cm}^3$ range, so that most available material is about 10-50 times more heavily doped than we need. Unfortunately, the budget level of this program precluded the possibility of getting custom-grown boules for this work, to meet the above specifications.

2.1.2 Junction Formation

Solar cells, with a p^+-n junction structure, were formed by direct p- diffusion into the bulk starting material. We believe that diffusion is a viable technique for GaAs provided that it can be carried out in an open tube system, and give reproducible results. We have previously shown (1,2) that the use of a zinc-doped oxide source, capped with a layer of phosphosilicate glass (PSG), allows this to be accomplished. The details of this process are now described.

Zinc-Doped Oxide Source: The source of zinc for formation of p-n

diffused junctions is a chemically vapor deposited ZnO-SiO₂ layer, which can be used to give zinc diffusions at about 600C, having surface concentrations of $\approx 1 \times 10^{20} \text{ cm}^{-3}$ with abrupt profiles. This source can be easily removed in dilute BHF or dilute HCl, with no surface damage to the GaAs.

The oxide is deposited in a resistance heated, cold wall reactor with gas flow at normal to the substrate surface. The chamber is maintained at atmospheric pressure with reactant gases entering at the top and being exhausted out of the bottom. The ZnO-SiO₂ layer is formed by the simultaneous oxidation of diethylzinc (DEZ) and silane at 325C. The DEZ is contained in a stainless steel bubbler at room temperature, and transported to the chamber using argon as a carrier gas; this gas is also used for dilution in the system. Oxygen and silane are introduced through a separate port.

The relative flow rates were set to obtain minimum sheet resistivity in the diffusion process. In our system, satisfactory results were obtained with an argon flow rate of 4.6 l/min, a silane partial pressure of $6.5 \times 10^{-15} \text{ atm}$, an oxygen partial pressure of $5.3 \times 10^{-6} \text{ atm}$, and a DEZ partial pressure of $5.3 \times 10^{-3} \text{ atm}$. These conditions gave a growth rate of about 80 Å/min for the zinc-doped oxide source layer.

The ZnO-SiO₂ layer has a refractive index of 1.8 and a conductivity of about $20 \text{ ohm}^{-1} \text{ cm}^{-1}$. It is soluble in dilute HCl and dilute BHF yielding a clear GaAs surface after zinc diffusion.

Tin-Doped Oxide Source: Work with tin diffusion into p-GaAs was pursued, with the thought that the longer electron diffusion length would result in more efficient current collection. Deposition of a tin-doped oxide source was carried out in the same reactor system, but in a separate reaction chamber in order to avoid contamination problems. Here, tetramethyltin (TMT) was used as the liquid source chemical, and was held in the bubbler maintained at room temperature. The doped oxide source was grown by the pyrolysis of TMT in oxygen. A substrate temperature of 400C was used, with a typical growth rate of 125 Å/min. A layer of 1000 Å thickness was used in most of our experiments. Complete details of the process are not given here, since this work was discontinued, for reasons which will be given later in this report.

Phosphosilicate Glass (PSG) Cap Layer: The phosphosilicate glass (PSG) used as a cap for the zinc diffusions is a low phosphorous content oxide layer, deposited at atmospheric pressure by the simultaneous oxidation of PH_3 and SiH_4 on substrates heated to 325C, making the process compatible with that for the zinc oxide source deposition. The low phosphorus content was chosen so that the PSG can be retained as a cap layer on the cell, without the problem of moisture absorption associated with high phosphorus content material.

The flows were chosen so as to obtain deposition uniformity over a 1.5 inch diameter area, and growth carried out in the reaction rate controlled region of deposition. The flow rates were argon at 2.2 l/min SiH_4 at 2.1 cc/min (9.5×10^{-4} atm), PH_3 at .036 cc/min (1.6×10^{-5} atm), and oxygen at 18 cc/min (8.2×10^{-3} atm). The deposition rate

was approximately $180 \text{ \AA} \text{ } \overset{\circ}{\text{Å}}/\text{min}$ for these flow conditions.

A different composition was chosen for use as an encapsulating layer for the high temperature thermal treatments of GaAs. This had a higher phosphorus content, so as to prevent cracking of the PSG at the required annealing temperatures (600-900C), without leaving residues on the GaAs surface on removal. The flow rates were Ar at 2.2 $\text{Å}/\text{min}$, silane at 3.0 cc/min (1.4×10^{-3} atm), phosphine at 0.23 cc/min (1.0×10^{-4} atm) and oxygen at 22.6 cc/min (.01 atm). The deposition rate was about $300 \text{ \AA} \text{ } \overset{\circ}{\text{Å}}/\text{min}$ for these flow conditions.

Diffusions: Two separate diffusion furnace systems were set up---one for zinc and one for tin. These were relatively simple units, with a small (6"-9") flat zone, since all our work was carried out in open tube systems, with a flowing nitrogen gas ambient. Zinc diffusion cycles were at 600-650C for 5-10 minutes. Junctions of typically $400 \text{ \AA} \text{ } \overset{\circ}{\text{Å}}$ depth with surface concentrations of about $1 \times 10^{20} \text{ cm}^{-3}$ were used for the solar cells fabricated by this process.

Diffusions were performed into various n-type starting materials of concentrations in the range $5 \times 10^{16} - 5 \times 10^{17} \text{ cm}^{-3}$. Junction depths were found to be fairly uniform over a 1" wafer ($\approx \pm 5\%$) and relatively independent of background concentrations, because of the extremely steep nature of the diffusion front (1). For diffusions into epitaxially grown GaAs, the junctions were observed to be deeper, and junction depths were dependent on background concentration. No attempt was made to study this very interesting result, since it did not fit the requirements of this program.

The repeatability of zinc diffusions from the CVD source, from one run to another is to a variation of $\pm 15\%$ in junction depth.

The tin source consists of a mixture of SnO_2 and SiO_2 , which was formed by chemical vapor deposition in a system similar to that used for the zinc source. Tetramethyltin, held at 20C was used as the liquid organometallic source for tin, and silane was used as the source for SiO_2 . A 1000 Å layer of the doped oxide was grown at 400C by the simultaneous pyrolysis of these two reactants in oxygen. Argon was used as the carrier gas.

The tin source was next covered with a 2000 Å layer of PSG which was grown by the process described earlier. Here, however, a 400C substrate temperature was used since the growth rate of SnO_2 by this method falls off rapidly at lower temperatures. Additionally, a higher P_2O_5 content (10-15% by weight) was used to minimize stresses at the diffusion temperature (800C).

This PSG glass is somewhat hygroscopic. Consequently, it was removed after the diffusion step, and before any further processing was carried out.

The diffusion of tin, unfortunately, proceeds at a much slower rate than that of zinc. Thus, typical junctions requiring a 600C, 10 min. diffusion with zinc as the dopant, require 800C at 20 minutes with the tin source. Thus, the integrity of the GaAs surface is lost, and its electronic properties impaired, unless elaborate care is taken in growing the cap layer.

Measurements on these diffused layers indicated the presence of a 'dead' layer on the surface which impaired cell performance. Although elaborate procedures were developed for its removal, the cell

performance was generally quite poor. As a result, the work was discontinued for this application, and our effort focussed on the p^+-n bulk solar cell.

2.1.3 Contacts and Patterning

To form an ohmic contact to the back surface of the cell, a 500 Å layer of Au-Ge, at the eutectic composition, was evaporated onto the back surface. This was then alloyed in forming gas at 450°C for a 2 minute duration. An additional 2500 Å thick layer of gold was electroplated onto the back contact to produce a low resistance metallic layer which was a convenient contact for measurement purposes.

The grid pattern for the ohmic contact to the top face of the cell was defined by conventional photolithographic techniques, using positive photoresist. The pattern was etched through the oxide layers using a dilute buffered hydrofluoric acid solution (1:10 = BHF:H₂O by volume). About 2 microns of gold was then electroplated on to the exposed p^+ surface. No alloying of this front contact was necessary due to the high surface concentration ($\approx 1 \times 10^{20} \text{ cm}^{-3}$) of the diffused p^+ layer.

The gold plating was carried out in electroplating solution using a platinum anode and a gold plated nail as contact to the GaAs as cathode.

The cell area was delineated in another photolithographic step, where the oxide and then the p^+ layer surrounding the cell area were removed by etching in dilute BHF followed by a room temperature Caro's etch (5:1:1 = H₂SO₄:H₂O₂:H₂O by volume) respectively.

The cell pattern consists of 10 fingers, 100 μm wide and 5 mm long, with a separation of 1mm, connected by a grid 300 μm wide. A bonding pad of 1mm x 1mm is provided for probing or bonding purposes. The cell area is 0.529 cm^2 , and theoretically calculated series resistance for this structure 0.5 ohms.

Another mask was designed, and cells fabricated for concentrator applications. This structure has a 32 finger pattern, with fingers 25 μm wide and 4.65 mm long, at a separation of 0.33 mm, connected by a grid 300 μm at one end and an additional grid 100 μm wide at the other. The bonding pad is 1.1mm x 1.09mm. The cell area is 0.501 cm^2 and this structure has a theoretically calculated series resistance of 0.08 ohms.

2.1.4 Anti-reflective Coating

The anti-reflective coating used by these cells was an evaporated layer of Sb_2O_3 , formed after the delineation of the grid pattern and cell area. The refractive index of Sb_2O_3 is ≈ 2 and optimum thickness chosen $\approx 750 \text{ \AA}$ for this application. Here, the process consists of removing the deposited dopant source and cap oxide layers in dilute BHF, prior to the formation of the AR coating.

An alternative approach takes advantage of the fact that ZnO with refractive index ≈ 2 and SiO_2 with refractive index ≈ 1.46 can together be used to form a 2-layer AR coating.

The thickness of the ZnOSiO_2 source (ref. index ≈ 1.8) and PSG cap layer (ref. index ≈ 1.46) were chosen to be approximately 750 \AA and 3200 \AA respectively. The two layers are deposited in a single CVD run at 325C. They serve as the zinc diffusion source, mask for pattern

delineation, and are then retained as an effective AR coating for the cell.

2.1.5 Alternative Cell Fabrication

During the last year we have developed an alternative novel approach to cell fabrication. This approach takes advantage of the fact that the zinc oxide layer has a refractive index of about 1.8 and is thus suitable for use as the AR coating in a 750 Å thick layer. Moreover, PSG, with a refractive index of about 1.46, can be used as a second layer to form a 2-layer AR system. Consequently, a cell process has been developed where CVD layers of carefully controlled thickness are used. These layers serve as the mask in subsequent pattern delineation, are left in place for the final cell structure.

This approach has the following advantages. First, a single process forms the dopant source, the cap layer and the 2-layer AR coating. Next, the GaAs surface is not exposed at any point in the process. Thus, the chance for surface contamination is minimized.

A short paper on this approach, and its results, has been submitted to the referred journals. (See Appendix A).

2.2 Electrical Characterization and Device Simulation

Electrical characterization consisted of a variety of electrical measurements on finished p^+ -n junction cells, on Au-GaAs Schottky cells fabricated on the starting bulk material and on small p^+ -n junction diodes and Au-GaAs Schottky diodes. A computer program was developed for simulating the spectral response on the p^+ -n junction cells. The results of the simulation was compared to spectral response measurements

of finished cells in order to determine important device and material parameters. In this part of the report we summarize both the results of the measurements and of the simulation, since they have already been presented in several papers or thesis written during the program.

2.2.1 Electrical Measurements

Electrical measurements on small junction and Schottky barrier diodes consisted of the measurement of the dark $\ln I$ vs. V characteristics, the C vs. V characteristics in the reverse direction and DLTS measurements. The C vs. V characteristics were used for determining the doping of the bulk material before and after junction formation by zinc diffusion. The doping concentration of the bulk material was found to decrease by approximately 50% after the zinc diffusion. Our measurements indicate that the zinc diffusion had not only a compensating effect but also a gettering effect since the minority carrier diffusion length was found to increase after zinc diffusion. The improvement in the diffusion length varied from sample to sample by typically was found to increase from 0.2 microns to 0.5 microns.

DLTS measurements on the small area p^+-n and Au-GaAs diodes were consistent with the increase in diffusion length. The primary change on the DLTS spectrum was not so much the change on the concentration of traps but on the reduction in their capture cross-section. Typically the trap cross-section decreased by 2 to 3 orders of magnitude indicating that the zinc formed a defect complex with the trap present in the original material. It is well known that pairing of impurities in semiconductors often brings a decrease in the cross-section of the defect.

2.2.2 Solar Cell Measurements

Measurements on finished solar cells consisted of measurement of dark $\ln I$ vs. V characteristics, photovoltaic performance at 1 sun simulated AM1 illumination and spectral response between 400 and 900 nm. Measurement of the cell $\ln I$ vs. V characteristics was used for determining the ideality factor which was in the range of 1.4 to 1.6 and it was consistent with the measured cell fill factor. These results indicated that the cell series resistance did not degrade the cell fill factor.

Spectral response on finished solar cells were measured on a set-up consisting of a monochromator, a light chopper, a lock-in amplifier and an Apple II+ computer with an A to D converter for data acquisition. A series of computer programs were written for use with this system. The photon flux of the system was calibrated using an EG & G silicon photodiode whose spectral response had been calibrated against an NBS standard.

The use of the Apple II+ computer with the A to D converter for data acquisition allowed the determination of the external quantum efficiency in a very fast and accurate way. Furthermore a few computer programs were written which were used for calculating the internal quantum efficiency from the external one by taking into account the particular AR coating used in the cell under test.

Another set of spectral response measurements consisted of measuring the variation of the photocurrent with reverse bias at a fixed wavelength. This type of measurement was used for determining the diffusion length of the starting bulk material using Schottky barrier solar cells with a transparent Au contact. The diffusion length and surface recombination of the p^+-n diffused cells were determined from a

comparison of the measured internal quantum efficiency with the one obtained from a computer simulation model which we describe next.

2.2.3 Computer Simulation of Spectral Response:

A computer program was developed for calculating the internal quantum efficiency as a function of wavelength for the diffused p^+ -n junction cells. The cell was modelled as consisting of 3 regions: the top P^+ layer followed by the depletion layer formed by the p^+ -n junction and the quasi-neutral N region. The device and material parameters of the model were the thickness of the P^+ layer x_j , the surface recombination velocity S at the interface between the p^+ region and the AR coating, the diffusion length L_n of the electrons in the p^+ region, the width W of the depletion layer and the diffusion length of holes L_p on the quasi-neutral region. The mobility μ_n of the electrons in the p^+ region and of holes μ_p in the N-region were taken to be the ones corresponding to the doping in those regions. The thickness of the depletion layer W was determined from C-V measurements of small area diodes fabricated in the same wafer.

The model described had 3 adjustable parameters S , x_j and L_p . The values of these parameters was determined from the best fit of the calculated curve to the experimental measurements. The short wavelength response is determined mainly by x_j and S since the value of the diffusion length L_n of the minority carriers was larger than the thickness x_j of the p^+ region. The long wavelength response is determined by the junction depth x_j , the width of the depletion layer W and the Diffusion length of the minority carriers L_p in the N-region.

Typical values obtained for these parameters were $x_j = 0.1 \mu\text{m}$, $S = 5 \times 10^6 \text{ cm/sec}$, $W = 0.1 \mu\text{m}$ and $L_p = 1.4 \mu\text{m}$.

3. EDUCATIONAL AND PROFESSIONAL

Our work during this program has involved 5 students, of which 3 were at the Master's level and 2 at the Doctoral. The services of a post-doc were also utilized on a part-time basis, during the early phase of this program. Details of papers and presentations now follow:

"Photovoltaic Characteristics of Diffused P^+ -N Bulk GaAs Solar Cells", presented at the 16th IEEE Photovoltaic Specialists Conference, San Diego, California, September 28 - October 1, 1982.

"Diffused P^+ -N Solar Cells in Bulk GaAs", presented at the Space Photovoltaic Research and Technology Conference, NASA Lewis Research Center, Cleveland, Ohio, April 20-22, 1982.

"Fabrication of P^+ -N Junction GaAs Solar Cells by a Novel Method", by S. K. Ghandhi, G. Mathur, H. Rode and J. M. Borrego, letter submitted to the Solid State Electronics, (May, 1984). (APPENDIX A)

"Diffused Junction P^+ -N Solar Cells in Bulk GaAs I - Fabrication and Cell Performance", by I. Bhat, K. N. Bhat, G. Mathur, J. M. Borrego and S. K. Ghandhi, Solid State Electronics, Vol. 27, No. 2, pp. 121-125 (1984).

"Diffused Junction P^+-N Solar Cells in Bulk GaAs II- Device Characterization and Modelling", by R. Keeney, L. M. G. Sundaram, H. Rode, I. Bhat, S. K. Ghandhi and J. M. Borrego, Solid State Electronics, Vol. 27, No. 2, pp. 127-130 (1984).

"Heat Treatment of Bulk GaAs Using a Phosphosilicate Glass Cap", by G. Mathur, M. L. Wheaton, J. M. Borrego, (submitted to Journal Appl. Phys.). APPENDIX B.

The students listed at the beginning of this report conducted their academic program with partial support on this grant. These include:

1. L. M. G. Sundaram--Ph.D (DLTS Methods).
2. G. Mathur--Ph.D (in preparation) on Cell Processing and Defect Interactions in GaAs.
3. H. Rode--M.S. (Instrumentation for Electrical Characterization of Solar Cells).
4. R. Keeney--M.S. (Spectral Response Instrumentation for Solar Cells).

In addition, I. Bhat and K. N. Bhat (post-doc) were involved in the early phases of this program.

4. CONCLUDING SUMMARY

The work in this program has resulted in the exploration of diffusion techniques for the fabrication of GaAs solar cells. The open tube diffusion process used for these cells was developed to the point where cells with a junction depth of 400-500 Å were routinely fabricated. In addition, use of these techniques has been extended to

the fabrication of a cell in which the diffusion source and the cap layer are also used as a 2-layer AR coating. We have shown that this technique is eminently suited for p^+-n structures, using a zinc diffusion source, but not for n^+-p structures. We note that the p^+-n structure should have superior performance in concentrator applications where the series resistance of the bulk material is of crucial importance.

A detailed study of the effect of heat treatment of GaAs with a phosphosilicate cap was undertaken, since our process requires open tube diffusion with this cap material. This study has shown that gettering of deep lying acceptor impurities in GaAs is accomplished by means of this cap, resulting in an increase in electron concentration and in the lifetime.

We note that the main impediment to the use of this approach is in the starting material. Here, these two problems are that the bulk concentration is too high ($\approx 10^{17}/\text{cm}^3$) and that the hole diffusion length is relatively low. Extensive computer programming has shown that the main problem is in the starting resistivity. We believe that cells of up to 20% efficiency (AM0 at 1 sun) should be achievable if starting material were available with an electron concentration of $10^{16}/\text{cc}$ and a hole diffusion of 1 micron.

A P P E N D I X A

FABRICATION OF P⁺-N JUNCTION GaAs SOLAR CELLS
BY A NOVEL METHOD

by

S. K. Ghandhi

G. Mathur

H. Rode

J. M. Borrego

Electrical, Computer, and Systems Engineering Department
Rensselaer Polytechnic Institute
Troy, New York 12181

Letter Submitted to Solid State Electronics

May 1, 1984

REVISED
May 1, 84
S. K. Ghandhi

ABSTRACT

P⁺-N diffused junction GaAs solar cells have been successfully fabricated using a novel method in which the diffusion source, anti-reflective coating and protective cover layer are all formed in a single chemical vapor deposition run. The advantage of this process lies in its simple, low cost fabrication procedure and in the fact that the GaAs surface is protected throughout the fabrication procedure.

INTRODUCTION

Steady improvements in bulk GaAs materials have made possible the fabrication of diffused junction GaAs solar cells with good performance.

Although not as efficient as cells made in epitaxial substrates, cell efficiencies are sufficiently high so as to provide a viable alternative for this application. We have shown (1) that low cost p⁺n junction solar cells, using open tube zinc diffusion into GaAs from a chemical vapor deposited (CVD) source, can be made using a deposited zinc-doped oxide source and a phosphosilicate glass cap. These source and cap layers must be eventually removed, and followed by the subsequent deposition of an anti-reflective coating of Sb₂O₃ after the grid pattern has been defined.

This letter reports on a novel method for making these cells, with the formation of a diffusion source, an anti-reflective (AR) coating and a protective cover glass in a single CVD operation. This greatly reduces process steps; moreover, the technique has the advantage that the GaAs surface is kept protected during the entire operation.

DEVICE FABRICATION

These solar cells have been fabricated using n-type bulk GaAs substrates, with a donor concentration $3-5 \times 10^{17} \text{ cm}^{-3}$. Samples were cleaned and surface etched using standard techniques outlined earlier (1). The CVD oxides were then deposited in a single operation at 325 °C. First, a 750 - 800 °A layer of ZnO-SiO₂ was deposited by the simultaneous oxidation of diethyl-zinc and silane. Next, a 3200 °A layer of phosphosilicate glass (PSG) was deposited at the same temperature by the simultaneous oxidation of silane and phosphine,

without opening the system. After this fabrication step, the ZnO-SiO₂ layer serves as a zinc source for the open tube diffusion, whereas the PSG layer serves as an effective cap to prevent out-diffusion (2) of zinc during the thermal treatment. The zinc diffusion is carried out in a nitrogen ambient at 600 °C to form junctions, typically 400 °A in depth (2). An ohmic contact was formed to the back by evaporation of 500 °A of Au-Ge of eutectic composition, followed by alloying at 450 °C for 2 minutes in a N₂/H₂ ambient (80% N₂).

Conventional photolithographic techniques were used to etch the grid pattern through the oxide layer, after which 2 μm of gold was electroplated to the exposed p⁺ region to form the top contact grid. No alloying step was required, since a surface concentration of approximately $1 \times 10^{20}/\text{cm}^3$ is obtained by this diffusion process (2). The area of the cell was then defined photolithographically and mesa etching used to delineate the active cell area (0.5 cm²).

At this point, the cell structure is complete. The ZnO-SiO₂ layer, with a refractive index of 1.8, and the PSG layer (refractive index ≈ 1.46) together serve as a two-layer AR coating, with their respective thicknesses selected for optimum performance. Moreover, the PSG layer serves as a integral protective cover glass for the cell, obviating the need for additional protection (3). The device structure is shown in Figure 1.

SOLAR CELL CHARACTERISTICS

Solar cells of 0.5 cm² area, fabricated by this method in bulk n-type GaAs, typically have an open circuit voltage, $V_{oc} = 0.9$ V, short circuit current density, $J_{sc} = 19.3$ mA/cm², fill factor = 0.75 and efficiency = 13.0 under AM1 conditions (simulated with ELH lamp, checked against an NBS secondary standard). The n-factor of these cells as

determined from the $\log I$ vs. V measurements, was typically 1.4 to 2.0 and the calculated (4) series resistance of this cell was 0.5 ohms. This is similar to results obtained when cells were made in bulk GaAs by conventional processing techniques (1). Figure 2 shows the dark and illuminated V-I characteristics for a cell of this type.

Figure 3 shows the measured external quantum efficiency for this cell. Also shown is the external quantum efficiency curve for a diffused junction GaAs cell with a single layer AR coating of Sb_2O_3 , for comparison purposes.

CONCLUSION

This technique, which has been successfully used to fabricate p^+n diffused junction GaAs solar cells, has the advantage that the diffusion source, the anti-reflective coating, and the protective cover layer for the completed solar cell are all formed in a single operation. In addition to the obvious cost advantage of this approach, the number of process steps is kept to an absolute minimum and the gallium arsenide surface is not exposed at any point during the entire fabrication process. Thus, the process yield for this technique should be high.

ACKNOWLEDGEMENTS

The authors would like to thank A. Hayner for manuscript preparation. This work was supported by Grant No. NAG3-188, from the NASA-Lewis Research Center, Cleveland, Ohio. This support is gratefully acknowledged.

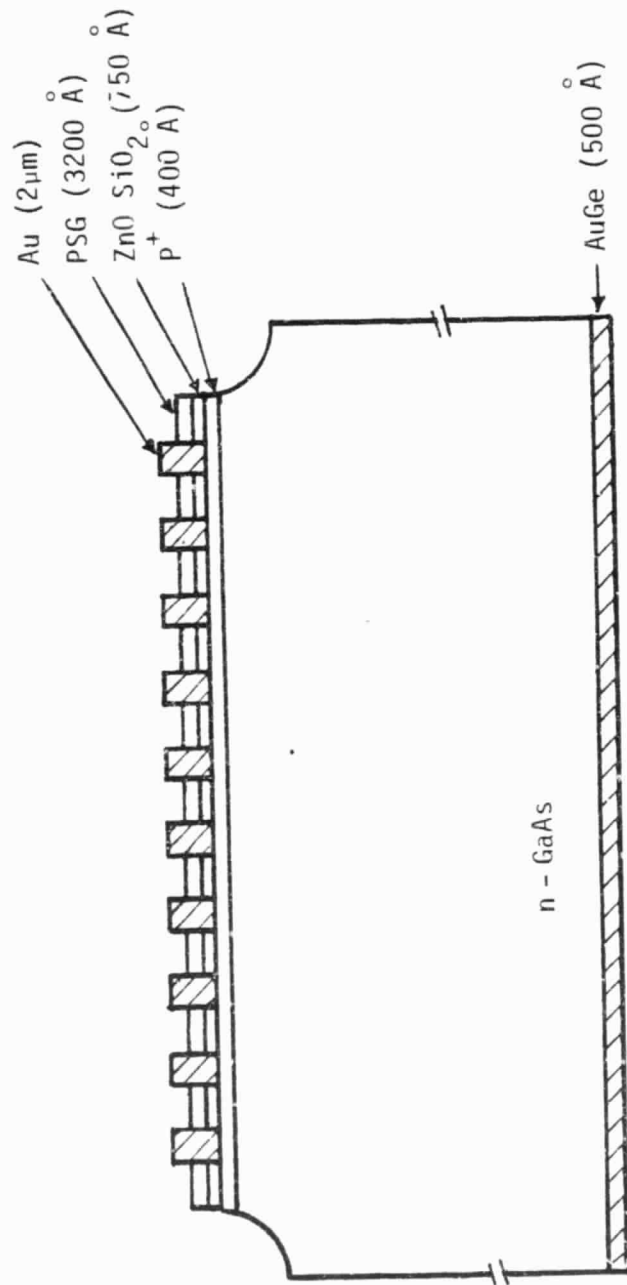
References

1. I. Bhat, K. N. Bhat, G. Mathur, J. M. Borrego, and S. K. Ghandhi, "Diffused Junction P⁺N Solar Cells in Bulk GaAs--Fabrication and Cell Performance", Solid State Electronics 27, 2, 121 (1984).
2. R. Jett Field, and S. K. Ghandhi, "An Open-Tube Method for Diffusion of Zinc into GaAs", J. Electrochem. Soc., 129, 7, 1567 (1982).
3. H. J. Hovel, "Semiconductors and Semimetals, Volume II", Academic Press, 1975.
4. R. J. Landy, "Theoretical Analysis of the Series Resistance of a Solar Cell", Solid State Electronics, 10, 765 (1967)

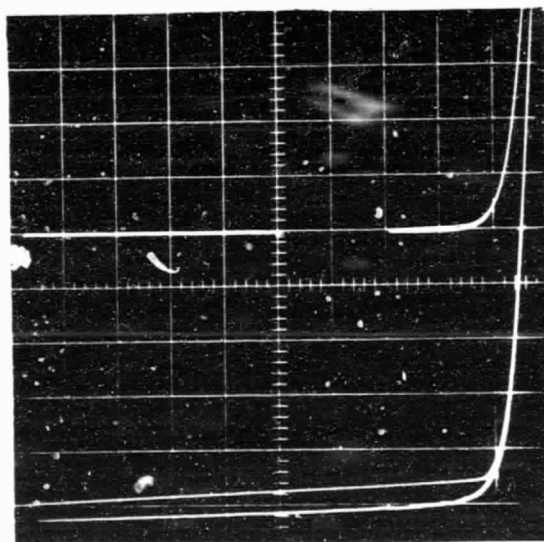
LEGENDS

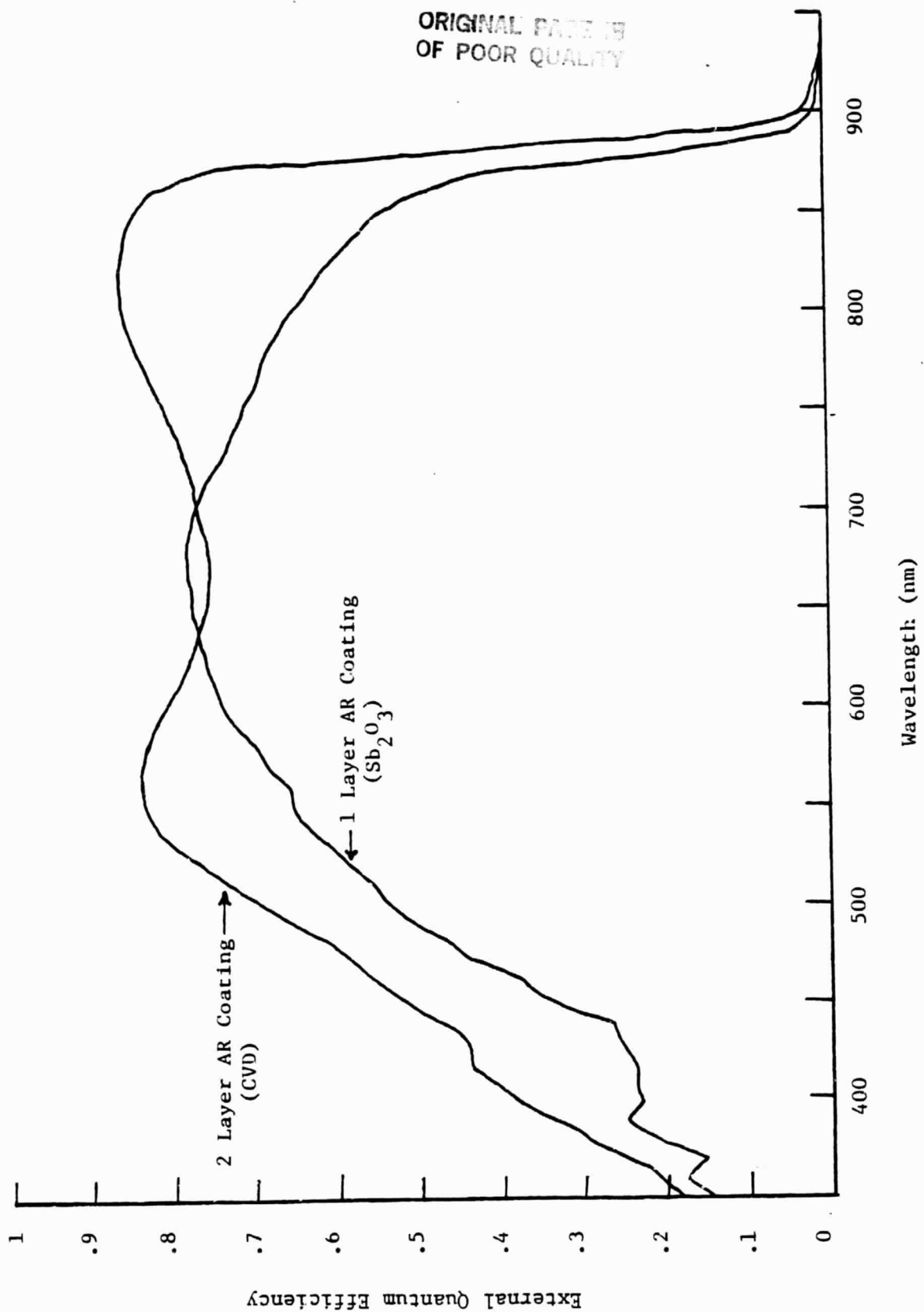
- FIGURE 1: Schematic cross-section of the p^+ -n diffused junction GaAs solar cell.
- FIGURE 2: V-I characteristics of a typical p^+ -n diffused junction GaAs solar cell under dark and AM1 illumination conditions. The scales are 2 mA/div. for the current and 0.2V/div. for the voltage.
- FIGURE 3: External Quantum Efficiency of typical cells with the two-layer AR coating and with a single-layer AR coating of Sb_2O_3 .

ORIGINAL PAGE 2
OF POOR QUALITY



ORIGINAL PAGE 3
OF POOR QUALITY





A P P E N D I X B

HEAT TREATMENT OF BULK GaAs USING A PHOSPHOSILICATE GLASS CAP

G. Mathur

M. L. Wheaton

J. M. Borrego

*S. K. Ghandhi

Electrical, Computer, and Systems Engineering Department

Rensselaer Polytechnic Institute

Troy, New York 12181

Submitted to the Journal of Applied Physics

October 22, 1984

*Point of Contact (518) 266-6085

ABSTRACT

N-type bulk GaAs crystals, capped with chemically vapor deposited phosphosilicate glass, were heat treated at temperatures in the range of 600°C to 950°C. Measurements on Schottky diodes and solar cells fabricated on the heat treated material show an increase in free carrier concentration, in minority carrier diffusion length and in solar cell short circuit current. The observed changes are attributed to a removal of lifetime reducing acceptor-like impurities, defects or their complexes.

INTRODUCTION

Gallium arsenide has a number of unique properties, which makes it superior to silicon in many application areas. These include high speed field effect transistors and integrated circuits (1), and electro-optical devices such as solar cells (2) and light emitters.

A major problem area in GaAs device fabrication technology stems from the fact that it is a compound semiconductor which is sensitive to thermal processing. At temperatures above 637°C, GaAs suffers a preferential loss of its more volatile component (arsenic) with a resulting change in its stoichiometry. Impurities and point defects play an important role in the processing of GaAs single crystal materials and devices as well. These and their complexes, especially those which produce acceptor levels in GaAs, result in lower carrier concentration and minority carrier lifetime in n-type material, and play a significant role in determining the material properties from a device application viewpoint.

The use of phosphosilicate glass (PSG) for impurity gettering has been extensively used in silicon processing. The gettering of impurities or defects from epitaxial GaP, using this glass, has also been reported (3). In our study, we performed heat treatments on n-type single crystal bulk GaAs capped with PSG. Results of these heat treatments are described in this paper. Their implication to solar cells fabricated in bulk single crystal GaAs has also been investigated.

EXPERIMENTAL PROCEDURE

The n-type bulk single crystal GaAs wafers used in this study had carrier concentrations in the range of $5 \times 10^{16} \text{ cm}^{-3}$ to $5 \times 10^{17} \text{ cm}^{-3}$ with (100) orientation. Substrates included silicon-doped boat grown crystals (from Laser Diode), and tellurium-doped LEC wafers (from Materials Research Limited). The samples were degreased sequentially in trichloroethylene, acetone and methanol and then chemically etched for 3 minutes in Caro's etch ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 5:1:1$ by volume). They were then encapsulated on both sides with a 5000 Å thick layer of chemically vapor deposited phosphosilicate glass (PSG). The PSG caps were deposited by the simultaneous oxidation of silane and phosphine at 325°C . The silane and phosphine used were obtained as a 3.0% mixture in argon (from Matheson Gas Products) and a 0.1% mixture in argon (from Air Products Incorporated) respectively. Argon (from Air Products Incorporated) was used as the carrier gas in this system. The reaction chamber was a cold wall enclosure with a resistance heated susceptor, operated at atmospheric pressure. The reactants were introduced at the top and exhausted from the bottom of the chamber.

The flow rates of the gaseous species were chosen to obtain PSG layers with 15 to 25% P_2O_5 content by weight. This is the desirable composition range required to minimize the interfacial stress between the oxide and the substrate (4). PSG layers of this thickness and composition have expansion coefficients suitably matched to GaAs and can withstand heat treatments in the required experimental range without any sign of cracking. The argon flow was maintained at 2.2 liters/min. Typical partial pressures for the reactant gases were 1.3×10^{-3} atm.

for silane, 1.0×10^{-4} atm. for phosphine, and 1.0×10^{-2} atm. for oxygen.

The heat treatment cycles were performed in an open tube furnace in flowing nitrogen gas (from Air Products Incorporated) in the temperature range of 600°C to 950°C. Following the anneal the PSG was removed in dilute buffered hydrofluoric acid.

In a number of cases, especially those where heat treatment was carried out for the longer times and at the higher temperatures, there was visual evidence of damage to the surface of the GaAs. This damage was removed in all cases by etching the samples to a depth of 2 μm . Subsequent electrical measurements were made on test structures fabricated after removal of these layers.

The variation of carrier concentration with depth was studied by successive non-destructive C-V measurements and etching steps. These measurements were taken by using a mercury probe to make Schottky contacts to the samples. The etch steps were done with Caro's etch ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 5:1:1$ by volume).

Finally, Au-GaAs Schottky test structures were fabricated on the samples, after removal of about 10 μm of the surface. Ohmic contacts were made to the back by vacuum evaporation of 500 Å of Au-Ge of eutectic composition, followed by annealing in a N_2/H_2 gas mixture at 450°C for 2 minutes. Next, the samples were given a dip in dilute HCl ($\text{HCl}:\text{H}_2\text{O} = 1:1$ by volume) prior to evaporation of the Schottky contacts. An array of small area ($2.21 \times 10^{-3} \text{ cm}^2$) Schottky diodes was made by vacuum evaporation of 500 Å thick gold dots through a metal mask onto the front surface. C-V measurements at 1 MHz were made on these diodes to obtain carrier concentration data.

Schottky solar cells were also fabricated by vacuum evaporation of 60 Å thick gold dots, 0.11 cm^2 in area, on the small dot array, with the smaller (thicker) gold dots serving as contacts. The short circuit current generated by these cells, under conditions of constant illumination provided a comparative measure of the change in diffusion length obtained by this heat treatment.

The minority carrier diffusion length was determined by measurement of the relative photoresponse of these Schottky solar cells at a single wavelength, as a function of depletion layer width (5). This technique is based on the fact that the normalized photocurrent for monochromatic illumination is a function of absorption coefficient, depletion width and diffusion length for high absorption coefficient materials such as GaAs. In this method, the photocurrent is measured as a function of reverse bias voltage at a single wavelength. The depletion width at corresponding reverse bias voltages is determined by capacitance voltage measurements. The diffusion length can be calculated from this data, since the absorption coefficient of GaAs is known. Non-annealed control samples, cut from the same wafer, were used for comparison purposes in all cases.

RESULTS

Heat treatment of n-type bulk single crystal GaAs was performed at different annealing temperatures in the 600°C - 950°C range, for a duration of 1 hour. Removal of the cap after annealing yielded a clean shiny surface for temperatures below 900°C and a shiny discolored skin on samples annealed above 900°C .

The depth of damage increased with increasing temperature, as would be expected for surface deterioration resulting from lattice defects generated at the PSG-GaAs interface. Based on reported diffusion data for vacancy defects in GaAs (6), we estimate that vacancies diffusing in from the interface would be within the top 1.5 μm for all the heat treatment cycles performed. At 950°C for a 1 hour duration, the estimated values for \sqrt{Dt} for the vacancies of gallium and arsenic are 1.3 μm and 3075 Å respectively. Chemical damage, from a reaction between the PSG and GaAs is also possible. Damage of this type was removed in all cases before electrical measurements were made to determine material properties. Typically, the removal of about 0.15 μm of the surface in the case of heat-treatments at 600°C, and about 1.5 μm for the 940°C anneal resulted in surfaces on which non-leaky Hg-GaAs Schottky diodes could be made for mercury probe tests. Carrier concentration values were obtained by analysis of the $1/C^2$ versus V data taken on these Schottky diodes. The carrier concentrations at different depths from the surface for the different heat treatment cycles show that uniform material properties were reached after removal of about 2 μm of material in all cases.

Figures 1 and 2 illustrate the variation of carrier concentration versus heat treatment temperature for experiments performed on n-type GaAs. These figures show an apparent increase in the electron concentration on annealing at the higher temperatures, and a slight fall at the lower temperatures. Furthermore, the carrier concentration change shows an increasing trend with increase in annealing temperature. All measurements were made at depths of more than 2.0 μm .

Schottky diodes and Schottky barrier solar cells were fabricated on the samples after removal of the damaged surface layers. The hole diffusion length, L_p , was measured using these devices, by the technique described earlier (5). Figures 3 and 4 illustrate the variation in L_p in the material as a result of 1 hour heat treatments at different temperatures. Removal of some lifetime killing impurity, defect or complex at the higher temperatures is clearly indicated in this data.

Figures 5 and 6 show the normalized short circuit current (I_{sc}) of the solar cells as a function of annealing temperature. The increase in I_{sc} together with an increase in carrier concentration and L_p , also indicates a removal of compensating, lifetime reducing acceptors from the material.

DISCUSSION

An analysis of what is occurring in the GaAs on heat treatment must begin with a model of the starting material. Bulk GaAs material is known to contain a significant concentration of transition metal impurities which are present in its starting constituents. These are the principal causes for low lifetime, since they are deep acceptor levels. V_{Ga} -donor complexes are also present in n-type GaAs as deep acceptors. Shallow acceptors may also be present, especially in silicon-doped material, due to the amphoteric nature of this dopant in GaAs. Since the material is relatively heavily doped n-type GaAs, with typical carrier concentrations of $1 \times 10^{17} \text{ cm}^{-3}$, we assume that it consists primarily of ionized shallow donor impurities, in addition to ionized acceptors, both deep and shallow.

An increase in n , concurrent with an increase in L_p implies a reduction in the ionized acceptor concentration. This reduction is possibly due to annealing out of acceptor-like impurities, defects or their complexes, or to gettering of impurities or defects which produce deep acceptor levels in the material.

In order to ascertain the actual mechanism of deep acceptor reduction, samples of similar material were heat treated without a cap for 1 hour in a 5 torr overpressure of arsine at 900°C. The system used was a cold wall epitaxial reactor with an R.F. heated graphite susceptor, which has been described elsewhere (7). A 10% mixture of arsine in hydrogen (from Air Products Incorporated) was used to maintain the overpressure of arsine. Hydrogen (from Air Products Incorporated) was palladium purified, and used for dilution and purging. Test devices, fabricated after removal of 20 μm of the surface, showed a 3% increase in n (and an increase in L_p) in the Si-doped GaAs as compared to a 10% increase in the presence of a PSG cap layer. The Te-doped GaAs experienced a 13% reduction in n (and a decrease in L_p), whereas heat treatment with a PSG cap gave a 10% increase in n and an increase in L_p . From these results, we conclude that the observed changes in the capped annealing experiments are primarily due to gettering by the PSG, and not due to the heat treatment alone.

Transition metal impurities, and their complexes, usually exhibit deep acceptor levels in GaAs (8,9). Moreover, they are fast diffusers and can rapidly diffuse to the surface at the temperatures and time durations used. The gettering of these impurities by PSG could account for the observed increase in n and L_p on heat treatment.

A slight reduction in n is observed at the lower annealing temperatures, typically below 800°C. It is probable that this drop is due to the introduction of contaminants from the PSG cap itself. These contaminants, which are fast diffusers in GaAs, are probably gettered at the higher temperatures (>800°C) together with impurities in the as-purchased bulk material. Photoluminescence spectra, taken on material annealed at 600°C for 30 minutes, showed the appearance of a new peak at 1.30 eV in Te-doped material, and a shift of the 1.20 eV peak to 1.26 eV in Si-doped material. This effect, which has been attributed to the Cu_{Ga} -donor complex (10), is however not seen in material annealed at 800°C. Based on diffusion studies on copper doping in GaAs (11), the estimated \sqrt{Dt} for copper at 600°C for 30 minutes is about 2mm. This strongly supports the presence of copper as a contaminant from the PSG, which results in acceptor levels in the GaAs on heat treatment at low temperatures.

The larger drop below the control values observed in the Te-doped samples as compared to the Si-doped samples could possibly arise from the different site incorporation of tellurium donors (on As sites) and silicon donors (on Ga sites) in GaAs crystals. This would result in a difference in the extent of the donor-copper interaction, the effect being more pronounced in the Te-doped material. It would also explain the observation of a dip below the control value of L_p in the Te-doped samples, which was not observed in the Si-doped samples.

It is found that the observed gettering effects are stronger in material with higher carrier concentration and lower minority carrier diffusion length. Thus, the effect of this gettering treatment depends on the quality of the starting material, and would be expected to be

larger in poorer quality substrates.

The photogenerated current for the Schottky solar cell is given by the expression (5):

$$J_p(\lambda) = -q N(\lambda) T(\lambda) \left[1 - \frac{\exp[-\alpha(\lambda) W]}{1 + \alpha(\lambda) L_p} \right]$$

where $N(\lambda)$ is the incident photon flux, $T(\lambda)$ is the transmittance of the upper layer, $\alpha(\lambda)$ is the absorption coefficient, L_p is the hole diffusion length and W the depletion layer width. The short circuit current (I_{sc}) of such a cell with 60 Å of Au, and no anti-reflective coating, was calculated by integrating over the 0.4 μm to 1.0 μm range of wavelength. The theoretically calculated values for the normalized short circuit current for the samples were found to be consistent with these measurements. There is an increase of about 12-13% in I_{sc} for cells made on GaAs which was previously heat treated at 940°C for 1 hour with a PSG cap. Computer simulation and analysis of the solar cell photogenerated current shows that, for these devices, I_{sc} is more sensitive to the changes in L_p as compared to changes in n . In addition the variations in I_{sc} with L_p , and with n , can be expected to be larger for material with shorter L_p and higher n respectively.

CONCLUSIONS

It is shown that heat treatment of bulk n-GaAs using PSG caps results in removal of lifetime reducing acceptors, effecting the carrier concentration and minority carrier diffusion length in the material. The extent of these changes would depend on the quality of the starting

material. The implication to solar cell applications has been illustrated by the fabrication of Schottky solar cells on these heat treated samples.

ACKNOWLEDGEMENTS

The authors would like to thank A. Hayner for manuscript preparation. This work was supported by Grant No. NAG3-188, from the NASA-Lewis Research Center, Cleveland, Ohio. This support is gratefully acknowledged.

REFERENCES

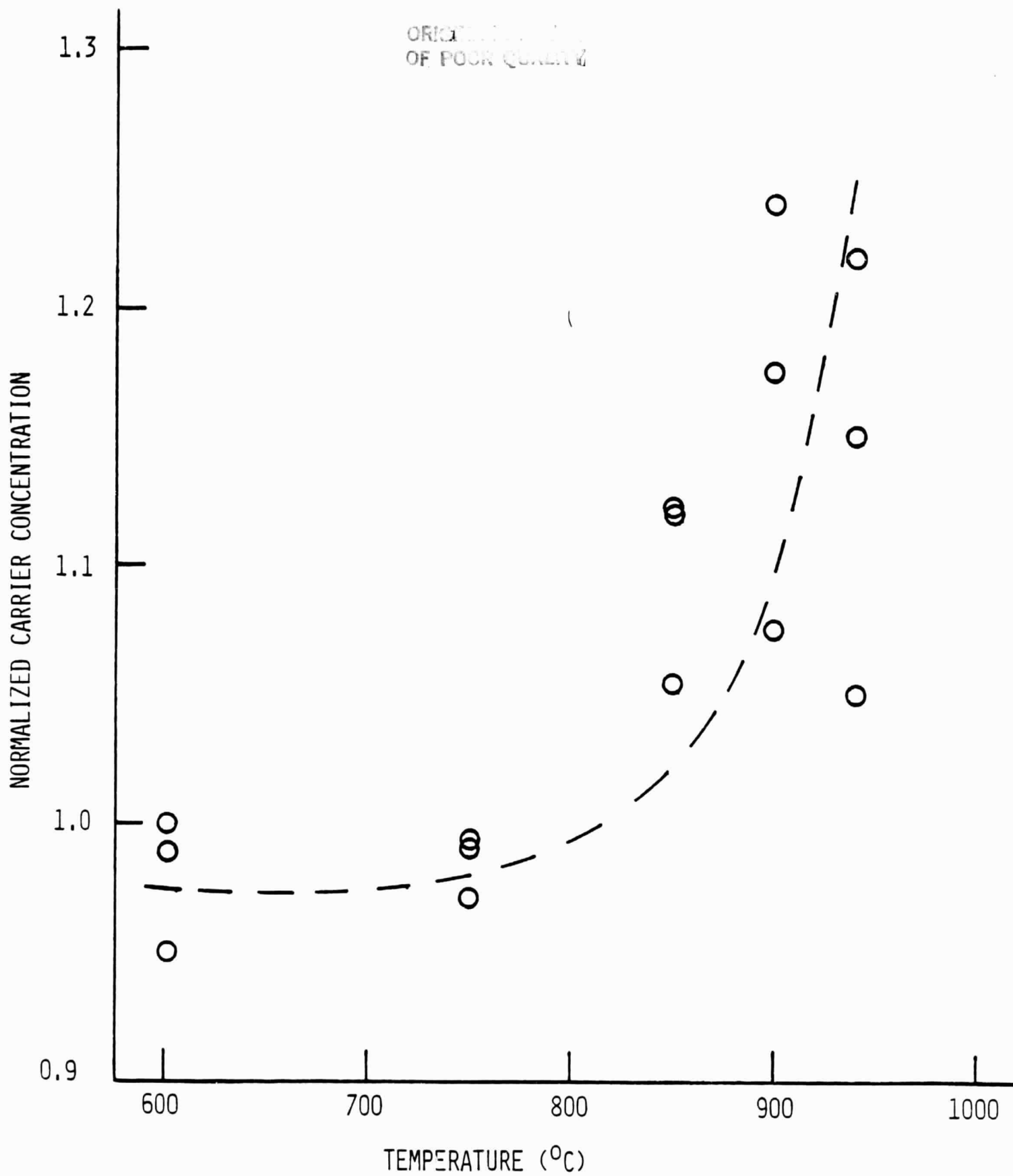
1. R. D. Fairman, R. T. Chen, J. R. Oliver, D. R. Chen, IEEE Trans. Electron Dev. ED-28, 2, 135-140 (1981).
2. I. Bhat, K. N. Bhat, G. Mathur, J. M. Borrego and S. K. Ghandhi, Solid State Electron. 27, 2, 121-125 (1984).
3. B. W. Wessels, Electron. Lett. 15, 23, 748-749 (1979).
4. B. J. Baliga and S. K. Ghanani, IEDM Technical Digest, 256-258, (1973).
5. R. J. Lender, S. Tiwari, J. M. Borrego and S. K. Ghandhi, Solid State Electron. 22, 213-214 (1979).
6. S. Y. Chiang and G. L. Pearson, J. Appl. Phys. 46, 2986-2991 (1975).
7. D. H. Raep, Ph.D Thesis, Rensselaer Polytechnic Institute, Troy, New York (1982).
8. D. L. Partin, A. G. Milnes and L. F. Vassamillet, J. Electrochem. Soc. 126, 1581-1583 (1979).

9. D. L. Partin, A. G. Milnes, and L. F. Vassamillet, J. Electrochem. Soc. 126, 1584-1588 (1979).
10. H. Nakashima, Japan. J. Appl. Phys. 10, 1737-1738 (1971).
11. D. Shaw, Ed., Atomic Diffusion in Semiconductors, Plenum, New York, 1973.

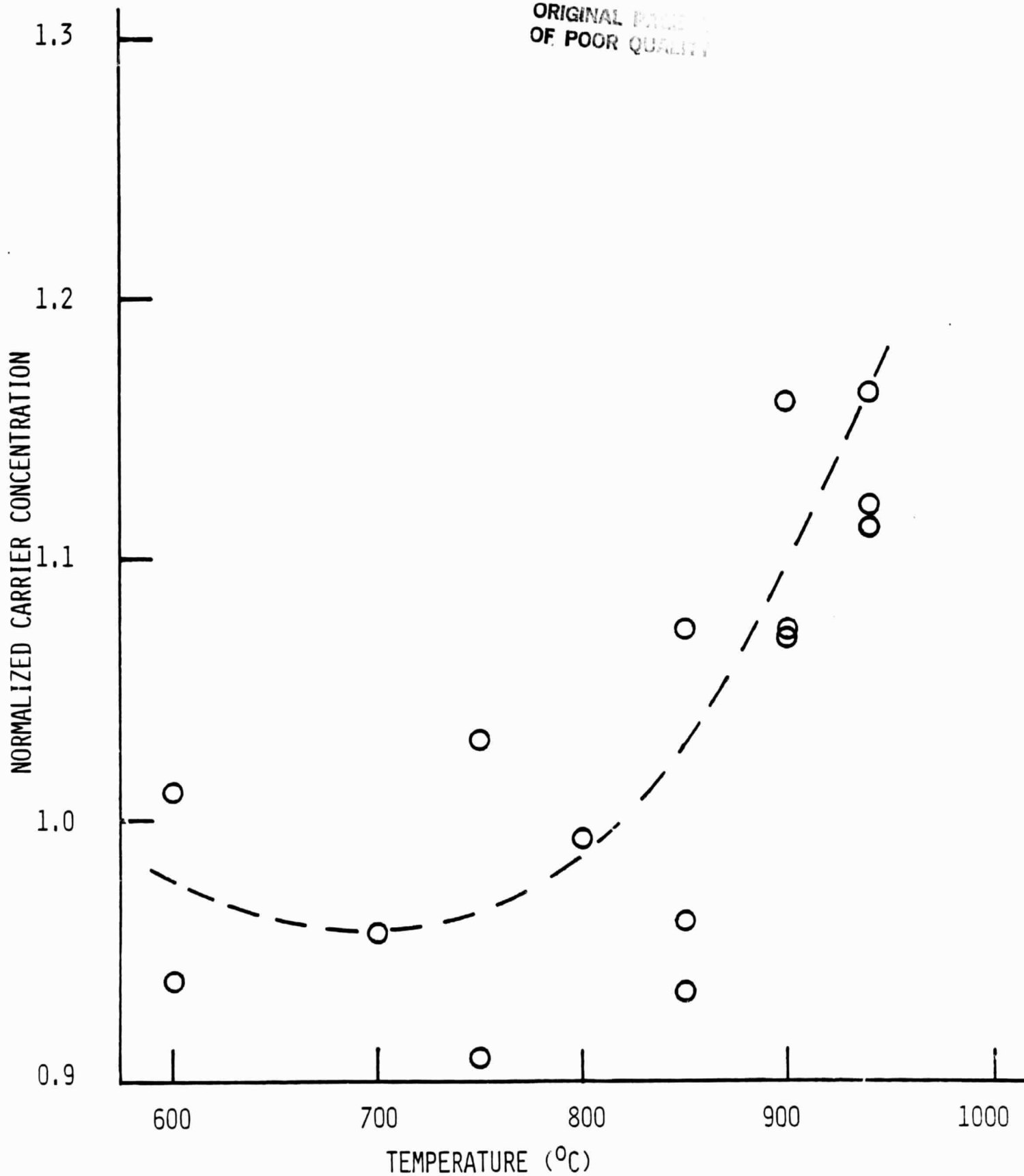
FIGURES

- Figure 1: Carrier concentration of Si-doped GaAs as a function of annealing temperature, after 1 hour anneal with a PSG cap. (Normalized to a control value of $2.8 \times 10^{17} \text{ cm}^{-3}$).
- Figure 2: Carrier concentration of Te-doped GaAs as a function of annealing temperature, after 1 hour anneal with a PSG cap. (Normalized to a control value of $7.8 \times 10^{16} \text{ cm}^{-3}$).
- Figure 3: Minority carrier diffusion length as a function of annealing temperature for Si-doped GaAs, after 1 hour anneal with a PSG cap. ($L_p = 0.42 \text{ } \mu\text{m}$ on non-annealed material).
- Figure 4: Minority carrier diffusion length as a function of annealing temperature for Te-doped GaAs, after 1 hour anneal with a PSG cap. ($L_p = .90 \text{ } \mu\text{m}$ on non-annealed material).
- Figure 5: Normalized short circuit current as a function of annealing temperature for Schottky barrier solar cells fabricated on heat treated Si-doped GaAs, after removal of $11 \text{ } \mu\text{m}$ of the surface. ($J_{SC} = 9.8 \text{ mA/cm}^2$ on control sample).

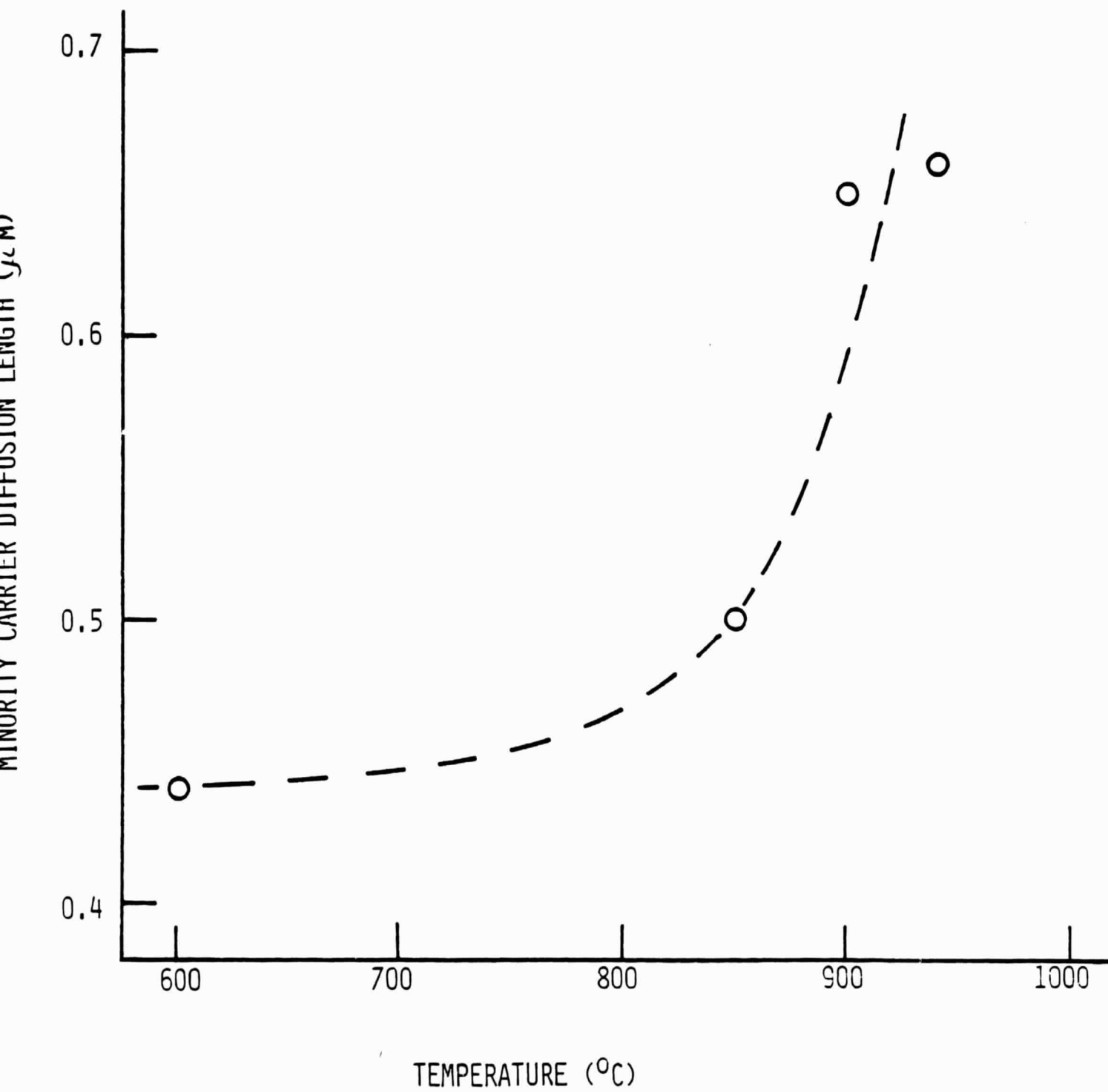
Figure 6: Normalized short circuit current as a function of temperature for Schottky barrier solar cells fabricated on heat treated Te-doped GaAs, after removal of 10 μm of the surface. ($J_{SC} = 12.3 \text{ mA/cm}^2$ on control sample).



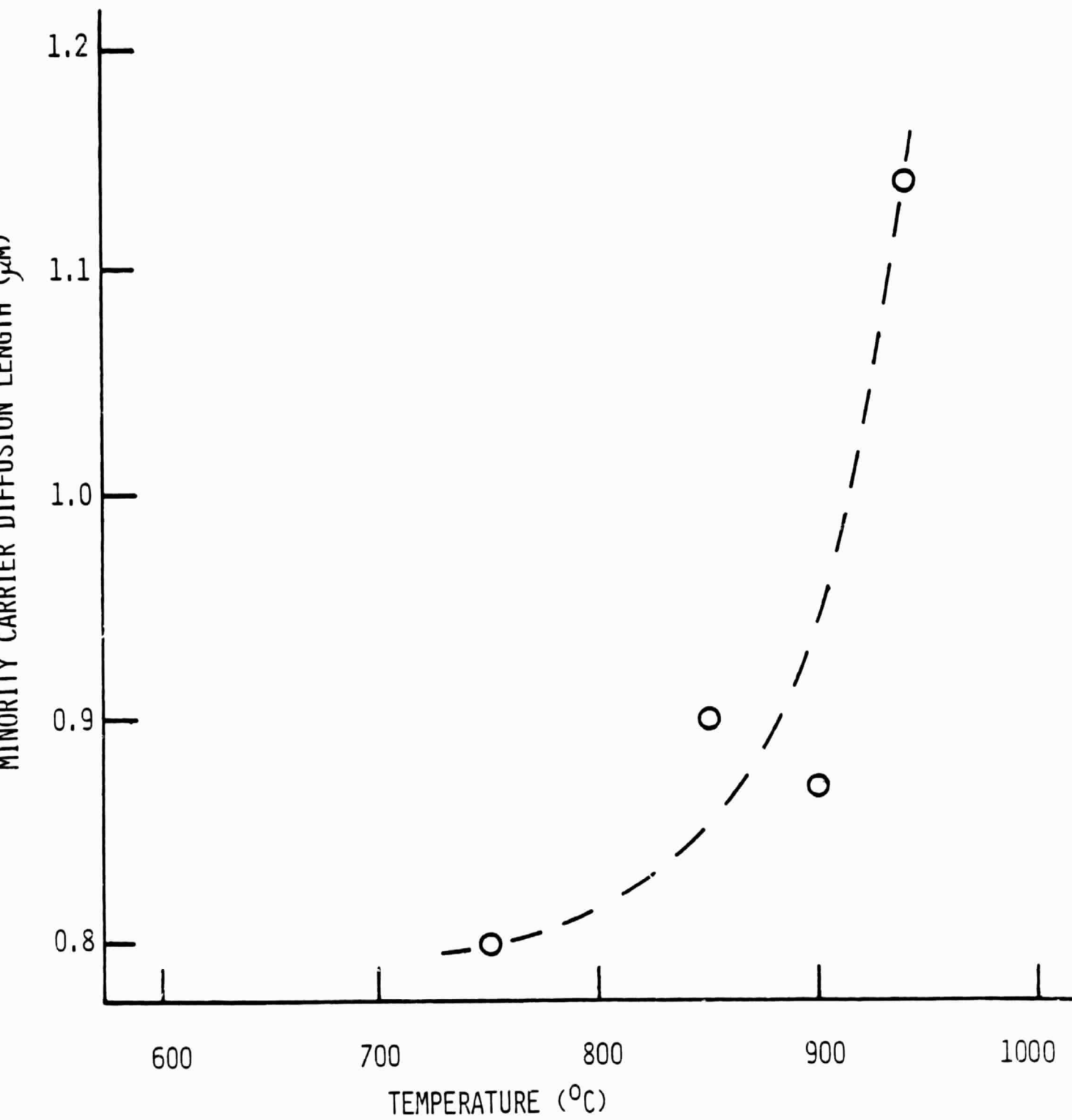
ORIGINAL PAGE
OF POOR QUALITY



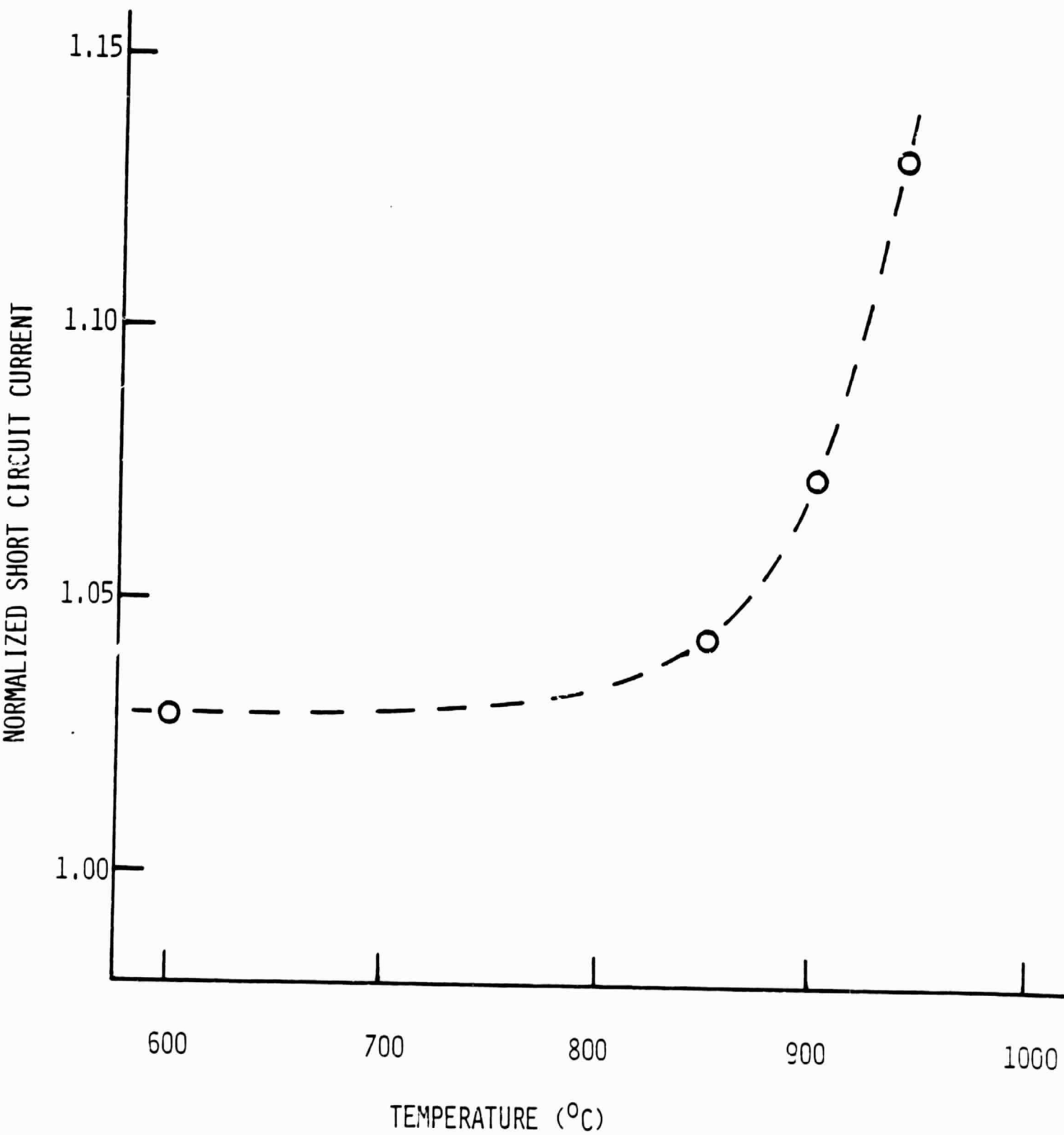
ORIGINAL PAGE IS
OF POOR QUALITY



ORIGINAL PAGE IS
OF POOR QUALITY



ORIGINAL FILM
OF POOR QUALITY



ORIGINAL PLOT IN
OF POOR QUALITY

NORMALIZED SHORT CIRCUIT CURRENT

